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Programming Concurrent Computers

1987 Workshop Schedule*

January 12-16
February 9-13
March 9-13

*Dates subject to change. Call (503) 629-7629 to verify.

ORDER NUMBER: 280179-003

"Programming Concurrent Computers" is designed to provide students with the fundamental knowledge, strategies, skills, and tools needed to design and implement large and complex programs for the Intel iPSC™ family of concurrent computers.

In addition, skills and concepts taught are generally applicable to message-passing, concurrent computing environments of other manufacturers.

Course Description

This course consists of a 5-day intensive "hands-on" workshop environment. It consists of:

Lectures — Introduce the fundamental knowledge and strategies of concurrent programming relevant to the hypercube architecture of the iPSC concurrent computer. Given by an experienced staff trainer.

Guest Lectures — Provide details of topics of special interest to application programmers. Presented by Intel engineers and scientists.

Examples & Case Studies — Illustrate the concepts and strategies presented in the lectures. Presented by both the staff trainer and guest lecturers.

Hands-On Experience — The laboratory sessions, which consist of roughly 60% of the total workshop time, provide extensive hands-on use. These sessions let the student put the lecture material into practice.

Lab Assistance — In-house staff engineers and scientists provide expert assistance during all lab sessions.

Class Discussions — Provide a forum for analyzing special problems and for letting students share their experiences from different scientific and engineering fields.

Intended Audience

Scientists and engineers who have purchased an iPSC concurrent computer and want to quickly get up to speed in programming it effectively.

Scientists and engineers who are considering purchase of an iPSC computer for either research or application development and who want to obtain a detailed assessment of the machine before purchasing it.

Any person interested in learning how to program a large-scale parallel computer.

Prerequisites

Experience in FORTRAN or C programming in a scientific or engineering field.

Experience with XENIX or UNIX operating systems is highly desirable.

Experience in concurrent programming is not required or assumed.

Typical Student Comments

Workshop ratings given by students range from "good" to "excellent." Some typical comments:

"The lab covered the major points of using the system—I feel very confident I can write applications on the iPSC after this course."

"I usually have no trouble thinking of improvements, but for this workshop, don't change a thing!"

"[The lab exercises] offered an excellent opportunity to learn the parameters of the system calls *and* to learn the (or a) suggested structure to the programs that do the calling. I believe the problem solutions are the more important materials I've received from the course."

"The coupling of the lecture presentations with the laboratory exercises was outstanding. It provided reinforcement of the concepts; yet were not so complex that 'thrashing' became the primary 'product'."

"[Got to meet] the entire cast of hardware, software, applications people, and got detailed answers to questions and concerns by the people who are actually doing the design and engineering."

"I'd heard much good about the class...and it was all accurate."

Tuition

The cost of the workshop is $1095 per student and includes:

- Course workbook
- iPSC User's Guide
- iPSC Simulator Manual
- iPSC Dynamic Loader Manual
- Supplementary material

One training credit is given with the purchase of any model iPSC computer. Tuition for non-iPSC customers can be applied to the subsequent purchase price of an iPSC computer.

For More Information and Reservations

Call Kay Cikowski at (503) 629-7629, or write to:

Intel Scientific Computers
Training Center
15201 NW Greenbrier Parkway
Beaverton, OR 97006

Attn: Kay Cikowski

Class Schedule

Time	Monday	Tuesday	Wednesday	Thursday	Friday
8:00	Introduction	Basic Concurrent Concepts	Applied Concurrent Computation Techniques	Concurrent Symbolic Applications	System Administration
9:00	The iPSC computer	Program Design Steps and Strategies			
10:00	Programming Environment		A Case Study	The Message Passing System	Customer Support
11:00	System Calls	Programming Cycle		Performance Analysis	Wrap-Up
12:00	LUNCH				
1:00	LAB 1 Concurrent Programming Basics	LAB 2 Speed-Up Analysis	LAB 3 2-D Meshes	LAB 4 Rings	LAB 5 Timing Analysis
2:00					
3:00					
4:00					
5:00	OPEN				

Course Topics

1. Introduction
- Traditional Computational Models
- Disadvantages of Traditional Models
- Alternative Models
- The Hypercube Model
- Advantages/Limitations of the Hypercube

2. iPSC™ Concurrent Computer
- General Overview
- Hardware Architecture
- Software Architecture

3. iPSC Programming Environment
- XENIX
- Tools
- Extensions

4. iPSC System Calls
- Cube Manager System Calls
- Node System Calls

5. Programming Cycles
- Cube Manager Cycle
- Node Cycle
- Short Cuts

6. Basic Concurrent Processing Concepts
- Serial vs Concurrent Processing
- Speed-up vs Efficiency
- Coarse vs Fine Granularity
- Homogeneous vs Heterogeneous Processes
- Load Balancing
- Communications Overhead

7. Basic Design Steps and Strategies
- Partitioning Applications Into Processes
- Defining Inter-process Communication
- Topologies
- Mapping Processes Into Nodes
- Avoiding Pitfalls

8. Applied General Concurrent Computational Techniques
- Grid Space Techniques
- Long Range Interaction Techniques
- Combination Techniques
- Matrix Manipulation Techniques
- FFT Techniques

9. Debugging
- General Strategies
- Checkpoints
- Interpreting Run Time Errors
- Others

10. Optimizing Strategies
- Built-In Optimizations
- Communication Optimizing
- Computation Optimizing
- Data Structure Optimizing

11. System Administration
- Modifying The Number Of Users
- Maintaining Security
- Adding/Removing Peripherals
- Backing Up Files
- Troubleshooting
- Booting/Shutting Down System

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Printed in USA/SC6062/1186/3K/LC/AP/VJC
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